Claim Amendments

1. (currently amended) A phase selection unit for generating a recovered clock signal, the phase selection unit comprising:

a phase select signal generator for generating a plurality of phase select signals in response to a FWD (forward) signal and a BWD (backward) signal from a digital filter;

wherein said digital filter asserts said FWD signal if the phase of a SDIN (serial digital input) signal leads the phase of said recovered clock signal;

and wherein said digital filter asserts said BWD signal if the phase of said SDIN (serial digital input) signal lags the phase of said recovered clock signal;

a first multiplexer for inputting a predetermined number of given clock signals arranged in a predetermined phase order and for outputting a first output clock signal and a second output clock signal with said first and second output clock signals each being one of said given clock signals;

a first phase interpolator that receives said first and second output clock signals from said multiplexer to generate said recovered clock signal having a phase that is phase interpolated between the phases of said first and second output clock signals; ~~and~~

a multiplexer control circuit that controls said multiplexer to select one of said given clock signals for each of said first and second output clock signals, depending on whether said phase select signals indicates that said FWD signal is asserted or that said BWD signal is asserted such that the phase of said recovered clock signal generated from said phase interpolator increases when said FWD signal is asserted and decreases when said BWD signal is asserted and remains substantially constant when said FWD signal and said BWD signal are not asserted;

a second multiplexer for inputting said predetermined number of given clock signals and for outputting a third output clock signal that has a 180º phase shift from said first output clock signal and for outputting a fourth output clock signal that has a 180º phase shift from said second output clock signal; and

a second phase interpolator that receives said third and fourth output clock signals to generate a complementary recovered clock signal that has a 180º phase shift from said recovered clock signal and that has a phase that is phase interpolated between the phases of said third and fourth output clock signals.

2. (original) The phase selection unit of claim 1:

wherein said phase select signal generator is comprised of a plurality of bidirectional flip flops with each flip flop having an output signal that is a respective one of said phase select signals;

and wherein said bidirectional flip flops are coupled together in a loop such that said phase select signals are arranged in a predetermined order with a selected one of said phase select signals being asserted as a currently asserted phase select signal with the rest of said phase select signals not being asserted;

and wherein a prior one from said currently asserted phase select signal in said order of said phase select signals is asserted as a newly asserted phase select signal when said BWD signal is asserted;

and wherein a subsequent one from said currently asserted phase select signal in said order of said phase select signals is asserted as said newly asserted phase select signal when said FWD signal is asserted;

and wherein a currently recovered clock signal is one of a chosen clock signal of said given clock signals, a leading interpolated clock signal of said chosen clock signal, or a lagging interpolated clock signal of said chosen clock signal,

and wherein said leading interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent leading clock signal in said predetermined phase order of said given clock signals;

and wherein said lagging interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal

and the phase of an adjacent lagging clock signal in said predetermined phase order of said given clock signals;

and wherein when said currently recovered clock signal is said chosen clock signal, said multiplexer control circuit controls said multiplexer to select said chosen clock signal as said first output clock signal and to select said adjacent leading clock signal of said chosen clock signal as said second output clock signal, such that a newly recovered clock signal generated by said phase interpolator is said leading interpolated clock signal of said chosen clock signal when said phase select signals indicate that said FWD signal is asserted;

and wherein when said currently recovered clock signal is said chosen clock signal, said multiplexer control circuit controls said multiplexer to select said chosen clock signal as said second output clock signal and to select said adjacent lagging clock signal of said chosen clock signal as said first output clock signal, such that said newly recovered clock signal generated by said phase interpolator is said lagging interpolated clock signal of said chosen clock signal when said phase select signals indicate that said BWD signal is asserted;

and wherein when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, said multiplexer control circuit controls said multiplexer to select, as said first and second output clock signals, an immediately leading one of said given clock signals having a phase that leads said currently recovered clock signal by a least phase amount, such that said newly recovered clock signal generated by said phase interpolator is said immediately leading one of said given clock signals when said phase select signals indicate that said FWD signal is asserted;

and wherein when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, said multiplexer control circuit controls said multiplexer to select, as said first and second output clock signals, an immediately lagging one of said given clock signals having a phase that lags said currently recovered clock signal by a least phase amount, such that said newly recovered clock signal generated by said phase interpolator is said

immediately lagging one of said given clock signals when said phase select signals indicate that said BWD signal is asserted.

3. (original) The phase selection unit of claim 2, wherein a first one of said loop of said bidirectional flip flops is a set flip flop, and wherein the rest of said bidirectional flip flops are reset flip flops, such that the phase select signal corresponding to said first one of said loop of said bidirectional flip flops is asserted as said currently asserted phase select signal in response to a RST (reset) signal.

4. (original) The phase selection unit of claim 3, wherein said loop of said bidirectional flip flops is a closed loop with said first one of said loop of said bidirectional flip flops being coupled to a last one of said loop of said bidirectional flip flops.

5. (original) The phase selection unit of claim 1, further comprising:

a voltage controlled oscillator for generating said predetermined number of given clock signals sent to said multiplexer with any two adjacent given clock signals in said predetermined phase order of said given clock signals having a substantially same phase difference and with first and last given clock signals in said predetermined phase order of said given clock signals having said substantially same phase difference.

6. (canceled)

7. (original) The phase selection unit of claim 1, wherein said phase selection unit comprises part of a DPLL (digital phase lock loop) within a SERDES (serializer/deserializer) transceiver.

8. (currently amended) A phase selection unit for generating a recovered clock signal, the phase selection unit comprising:

means for generating a plurality of phase select signals in response to a FWD (forward) signal and a BWD (backward) signal from a digital filter;

wherein said digital filter asserts said FWD signal if the phase of a SDIN (serial digital input) signal leads the phase of said recovered clock signal;

and wherein said digital filter asserts said BWD signal if the phase of said SDIN (serial digital input) signal lags the phase of said recovered clock signal;

and wherein said phase select signals are arranged in a predetermined order with a selected one of said phase select signals being asserted as a currently asserted phase select signal with the rest of said phase select signals not being asserted;

and wherein a prior one from said currently asserted phase select signal in said order of said phase select signals is asserted as a newly asserted phase select signal when said BWD signal is asserted;

and wherein a subsequent one from said currently asserted phase select signal in said order of said phase select signals is asserted as said newly asserted phase select signal when said FWD signal is asserted;

means for generating said recovered clock signal having a phase that is phase interpolated between a first phase of a first output clock signal and a second phase of a second output clock signal; and

means for selecting each of said first and second output clock signals as one of a predetermined number of given clock signals arranged in a predetermined phase order, depending on whether said phase select signals indicate that said FWD signal is asserted or that said BWD signal is asserted such that the phase of said recovered clock signal increases when said FWD signal is asserted and decreases when said BWD signal is asserted and remains substantially constant when said FWD signal and said BWD signal are not asserted; and

means for generating a complementary recovered clock signal that has a 180º phase shift from said recovered clock signal and that has a phase that is

phase interpolated between the phases of third and fourth output clock signals, wherein said third output clock signal has a 180º phase shift from said first output clock signal, and wherein said fourth output clock signal has a 180º phase shift from said second output clock signal.

9. (original) The phase selection unit of claim 8:

wherein a currently recovered clock signal is one of a chosen clock signal of said given clock signals, a leading interpolated clock signal of said chosen clock signal, or a lagging interpolated clock signal of said chosen clock signal,

and wherein said leading interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent leading clock signal in said predetermined phase order of said given clock signals;

and wherein said lagging interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent lagging clock signal in said predetermined phase order of said given clock signals;

and wherein when said currently recovered clock signal is said chosen clock signal, said chosen clock signal is selected as said first output clock signal, and said adjacent leading clock signal of said chosen clock signal is selected as said second output clock signal, such that a newly recovered clock signal is said leading interpolated clock signal of said chosen clock signal when said phase select signals indicate that said FWD signal is asserted;

and wherein when said currently recovered clock signal is said chosen clock signal, said chosen clock signal is selected as said second output clock signal, and said adjacent lagging clock signal of said chosen clock signal is selected as said first output clock signal, such that said newly recovered clock signal is said lagging interpolated clock signal of said chosen clock signal when said phase select signals indicate that said BWD signal is asserted;

and wherein when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, an immediately leading one of said

given clock signals having a phase that leads said currently recovered clock signal by a least phase amount is selected as said first and second output clock signals, such that said newly recovered clock signal generated by said phase interpolator is said immediately leading one of said given clock signals when said phase select signals indicate that said FWD signal is asserted;

and wherein when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, an immediately lagging one of said given clock signals having a phase that lags said currently recovered clock signal by a least phase amount is selected as said first and second output clock signals, such that said newly recovered clock signal generated by said phase interpolator is said immediately lagging one of said given clock signals when said phase select signals indicate that said BWD signal is asserted.

10. (original) The phase selection unit of claim 9, wherein a first one of said phase select signals is asserted as said currently asserted phase select signal in response to a RST (reset) signal.

11. (original) The phase selection unit of claim 8, wherein said predetermined order of said phase select signals is a closed loop with a first phase select signal being adjacent a last phase select signal in said closed loop of said predetermined order of said phase select signals.

12. (original) The phase selection unit of claim 8, further comprising:

means for generating said predetermined number of given clock signals with any two adjacent given clock signals in said predetermined phase order of said given clock signals having a substantially same phase difference and with first and last given clock signals in said predetermined phase order of said given clock signals having said substantially same phase difference.

13. (canceled)

14. (original) The phase selection unit of claim 8, wherein said phase selection unit comprises part of a DPLL (digital phase lock loop) within a SERDES (serializer/deserializer) transceiver.

15. (currently amended) A method for generating a recovered clock signal, comprising:

generating a plurality of phase select signals in response to a FWD (forward) signal and a BWD (backward) signal from a digital filter;

wherein said digital filter asserts said FWD signal if the phase of a SDIN (serial digital input) signal leads the phase of said recovered clock signal;

and wherein said digital filter asserts said BWD signal if the phase of said SDIN (serial digital input) signal lags the phase of said recovered clock signal;

and wherein said phase select signals are arranged in a predetermined order with a selected one of said phase select signals being asserted as a currently asserted phase select signal with the rest of said phase select signals not being asserted;

and wherein a first one of said phase select signals is asserted as said currently asserted phase select signal in response to a RST (reset) signal;

and wherein a prior one from said currently asserted phase select signal in said order of said phase select signals is asserted as a newly asserted phase select signal when said BWD signal is asserted;

and wherein a subsequent one from said currently asserted phase select signal in said order of said phase select signals is asserted as said newly asserted phase select signal when said FWD signal is asserted;

generating said recovered clock signal having a phase that is phase interpolated between a first phase of a first output clock signal and a second phase of a second output clock signal; and

selecting each of said first and second output clock signals as one of a predetermined number of given clock signals arranged in a predetermined phase order, depending on whether said phase select signals indicate that said FWD signal is asserted or that said BWD signal is asserted such that the phase of said

recovered clock signal increases when said FWD signal is asserted and decreases when said BWD signal is asserted and remains substantially constant when said FWD signal and said BWD signal are not asserted.

16. (original) The method of claim 15:

wherein a currently recovered clock signal is one of a chosen clock signal of said given clock signals, a leading interpolated clock signal of said chosen clock signal, or a lagging interpolated clock signal of said chosen clock signal,

and wherein said leading interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent leading clock signal in said predetermined phase order of said given clock signals;

and wherein said lagging interpolated clock signal of said chosen clock signal has a phase that is an average of the phase of said chosen clock signal and the phase of an adjacent lagging clock signal in said predetermined phase order of said given clock signals;

the method of claim 15 further comprising:

selecting when said currently recovered clock signal is said chosen clock signal, said chosen clock signal as said first output clock signal, and said adjacent leading clock signal of said chosen clock signal as said second output clock signal, such that a newly recovered clock signal is said leading interpolated clock signal of said chosen clock signal when said phase select signals indicate that said FWD signal is asserted;

selecting when said currently recovered clock signal is said chosen clock signal, said chosen clock signal as said second output clock signal, and said adjacent lagging clock signal of said chosen clock signal as said first output clock signal, such that said newly recovered clock signal is said lagging interpolated clock signal of said chosen clock signal when said phase select signals indicate that said BWD signal is asserted;

selecting when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, an immediately leading one of said given

clock signals having a phase that leads said currently recovered clock signal by a least phase amount as said first and second output clock signals, such that said newly recovered clock signal is said immediately leading one of said given clock signals when said phase select signals indicate that said FWD signal is asserted; and

selecting when said currently recovered clock signal is one of said leading or lagging interpolated clock signals, an immediately lagging one of said given clock signals having a phase that lags said currently recovered clock signal by a least phase amount as said first and second output clock signals, such that said newly recovered clock signal is said immediately lagging one of said given clock signals when said phase select signals indicate that said BWD signal is asserted.

17. (canceled)

18. (original) The method of claim 16, wherein said predetermined order of said phase select signals is a closed loop with a first phase select signal being adjacent a last phase select signal in said closed loop of said predetermined order of said phase select signals.

19. (original) The method of claim 15, further comprising:

generating said predetermined number of given clock signals with any two adjacent given clock signals in said predetermined phase order of said given clock signals having a substantially same phase difference and with first and last given clock signals in said predetermined phase order of said given clock signals having said substantially same phase difference.

20. (original) The method of claim 15, further comprising:

generating a complementary recovered clock signal that has a 180º phase shift from said recovered clock signal and that has a phase that is phase interpolated between the phases of third and fourth output clock signals, wherein said third output clock signal has a 180º phase shift from said first output clock

signal, and wherein said fourth output clock signal has a 180º phase shift from said second output clock signal.

21. (original) The method of claim 15, wherein said recovered clock signal is an output of a DPLL (digital phase lock loop) within a SERDES (serializer/deserializer) transceiver.

22-30. (canceled)